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### (54) Communication bus system between processors and memory modules

(57) An apparatus (10) is provided for address and data distribution to memory modules (20). The apparatus (10) includes a controller (12) for controlling memory modules that comprises an optical transmitter (14) and a receiver (24). An optical cable (16) having a plurality of optical fibers (18) is connected to the optical transmitter (14) of the controller (12). A plurality of memory modules (20) are each connected to one of the optical fibers (18) and have a driver for transmitting data. A communication bus (22) is connected to the drivers of the memory modules (20) and to the receiver (24) of the controller (12). The controller (12) is operable to broadcast address and data information to the memory modules (20) via the optical fibers (18), and the memory modules (20) are operable to transmit data to the controller (12) via the drivers and the communication bus (22).

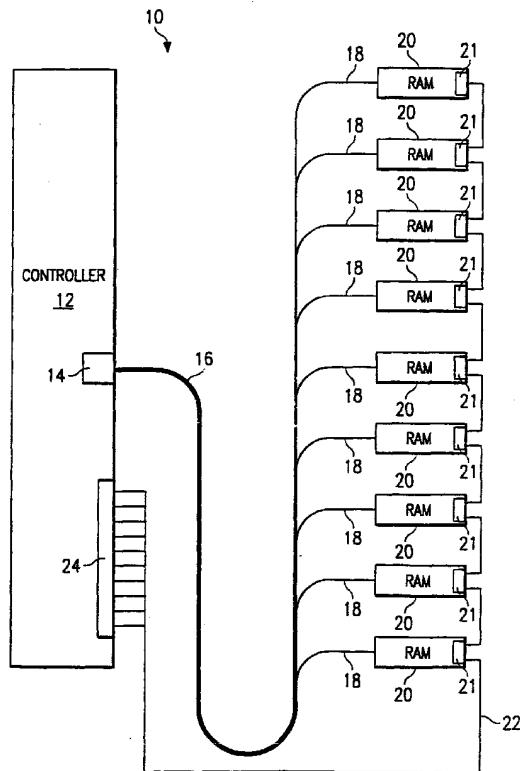


FIG. 1

**Description****TECHNICAL FIELD OF THE INVENTION**

This invention relates in general to the field of electronic devices, and more particularly to an apparatus and method for address and data distribution to memory modules.

**BACKGROUND OF THE INVENTION**

Communication between processors and main memory modules requires communication across a given physical bus length. Due to the physical bus length, there is an upfront latency produced by propagation time of signals across the bus. For example, a typical upfront latency may be 10 nanoseconds. As processing speeds increase to the 500 MHz range and above, a typical 10 nanosecond latency begins to cause problems. One conventional point-to-point communication protocol for increasing the speed of communication with memory modules is RAMLINK, which is defined by IEEE Standard 1596.4. However, it is desirable to reduce the upfront latency of communicating with memory modules without requiring the use of such a protocol.

**SUMMARY OF THE INVENTION**

Accordingly the present invention provides an apparatus and method for address and data distribution to memory modules that substantially reduce or eliminate problems and disadvantages of prior computer systems.

According to a preferred embodiment thereof, an apparatus is provided for address and data distribution to memory modules. The apparatus includes a controller for controlling memory modules that comprises an optical transmitter and a receiver. An optical cable having a plurality of optical fibers is connected to the optical transmitter of the controller. A plurality of memory modules are each connected to one of the optical fibers and have a driver for transmitting data. A communication bus is connected to the drivers of the memory modules and to the receiver of the controller. The controller is operable to broadcast address and data information to the memory modules via the optical fibers, and the memory modules are operable to transmit data to the controller via the drivers and the communication bus.

An advantage is that the use of an optical drive and optical fiber for communicating with memory modules and the use of low power drivers for return data in order both to reduce upfront latency and to provide a low power solution.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will now be further described by way of example, with reference to the accompanying

drawings in which:

**FIGURE 1** is a block diagram of a first embodiment of an apparatus for address and data distribution according to the teachings of the present invention; and

**FIGURE 2** is a block diagram of a second embodiment of an apparatus for address and data distribution according to the teachings of the present invention.

**DETAILED DESCRIPTION OF THE INVENTION**

**FIGURE 1** is a block diagram of an embodiment of

an apparatus, indicated generally at 10, for address and data distribution. Apparatus 10 includes a controller 12 that has an optical transmitter 14. An optical cable 16 is connected to optical transmitter 14 and includes a plurality of individual optical fibers 18. Individual optical fibers 18 are connected to associated memory modules 20. Memory modules 20 can be DRAM, SRAM or other types of memory modules used in electronic systems. Memory modules 20 are connected to controller 12 via a communication bus 22 to return data driven by low power drivers 21. Controller 12 includes a receiver 24 which receives communication bus 22 from memory modules 20.

In operation, controller 12 communicates with a processor or other components within a computer system in order to manage operation of the memory space provided by memory modules 20. In order to accomplish this function, controller 12 uses optical transmitter 14 to drive signals on cable 16 and fibers 18 to communicate address and data information to memory modules 20.

Communication bus 22 is driven by the low power drivers 21 on memory modules 20 to provide data back to controller 12 via receiver 24. In this manner, apparatus 10 provides high speed communication of address and data information from controller 12 to memory modules 20 in order to reduce upfront latency of communication with memory modules. If a read operation is performed, data is provided back to controller 12 using low power drivers 21 such that the apparatus 10 provides both reduced upfront latency and low power operation.

Conventional synchronous DRAMs (SDRAMs), for example, are capable of 100 MHz operation. It is contemplated that SDRAMs and other memory modules will be operated at 200 MHz and higher. Some conventional computer systems operate at 200 MHz and will soon operate at 300 MHz and higher. The bandwidth is improved substantially by synchronous DRAMs. However, the physical latency becomes relatively larger as the number of memory modules and speed increases. The conventional RAMLINK proposal is an interface protocol that does not address physical latency. Thus, the present invention provides advantages over conventional systems by broadcasting the address and data to the memory modules across high speed optical fiber.

The RAMLINK protocol can still be used, if desired, for the return of data to controller 12. Apparatus 10 reduces the additional input pin count of the memory modules to an optical receiver and a loaded output which can be a differential link from memory module to memory module as shown in FIGURE 2. Since the majority of the increase in physical latency is getting the address to the correct memory module, the apparatus 10 substantially reduces this address latency increase. As a trade-off, the output physical latency could also be reduced by also making it an optical drive and having a gather operation rather than a broadcast where all fibers would be terminated at one location. However, this would require more power than low power operation using low power drivers on the memory modules.

FIGURE 2 is a block diagram of an alternative apparatus, indicated generally at 20, for address and data distribution. As shown, controller 12 includes a transmit laser 14 which is connected to optical cable 16. Transmit laser 14 operates to transmit address and data optically to the various memory modules via optical cable 16. Data is returned from the memory modules differentially on differential lines 22 to a differential receiver 24. In this manner, the data returned from the memory modules can use a point-to-point communication protocol such as the RAMLINK protocol.

Although the certain embodiments have been described in detail, it should be understood that various changes, substitutions and alterations can be made thereto without departing from the spirit and scope of the teachings disclosed herein.

## Claims

1. An apparatus for address and data distribution to memory modules, comprising:

a controller for controlling memory modules comprising an optical transmitter and a receiver;  
an optical cable having a plurality of optical fibers, the optical cable connected to the optical transmitter;  
a plurality of memory modules, each connected to one of the optical fibers and having a driver for transmitting data; and  
a communication bus connected to the drivers of the memory modules and to the receiver of the controller; wherein the controller is operable to broadcast address and data information to the memory modules via the optical fibers; and the memory modules are operable to transmit data to the controller via the drivers and the communication bus.

2. The apparatus of Claim 1, wherein the driver of each memory module is a low power driver.

3. The apparatus of Claim 1 or Claim 2, wherein the driver of each memory module is an optical transmitter and the communication bus is formed from optical fibers.

4. The apparatus of any of Claims 1 to 3, wherein the communication bus comprises differential lines and the memory modules transmit data using a RAMLINK protocol.

5. A method for address and data distribution to memory modules, comprising:

10 connecting a controller for controlling memory modules and a plurality of memory modules with an optical cable having a plurality of optical fibers, such that the optical cable is connected to the optical transmitter of the controller; transmitting address and data information from the controller to the memory modules via the optical fibers; and transmitting data from the plurality of memory modules to the controller via a communication bus.

15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 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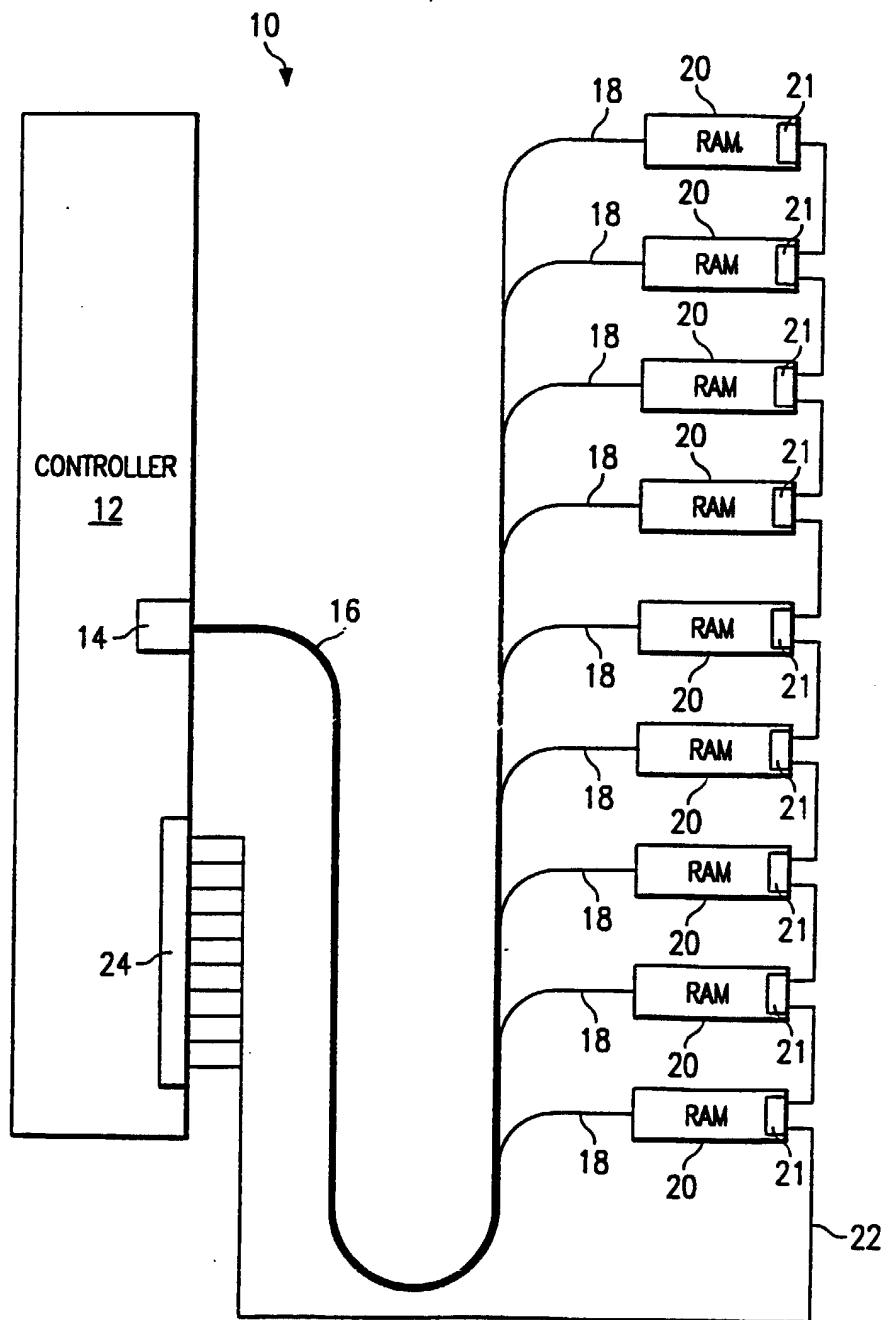


FIG. 1

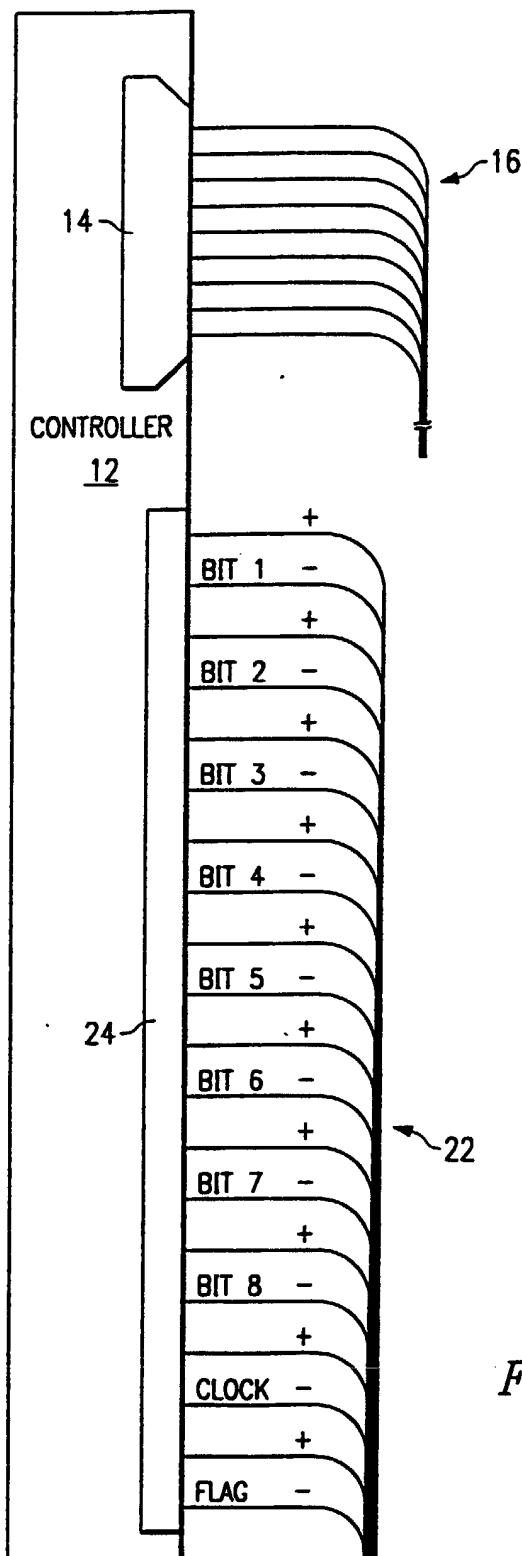


FIG. 2